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graph LR
    InputSignal[Input signal] --> FirstLevelShifter[First level shifter 100]
    OutputEnableSignal[Output enable signal] --> SecondLevelShifter[Second level shifter 110]
    FirstLevelShifter --> OutputDrivingUnit[Output driving unit 500]
    SecondLevelShifter --> OutputDrivingUnit
    OutputDrivingUnit --> OutputSignal[Output signal]
  
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The diagram shows a circuit with an input signal or output enable signal entering a block labeled 200. Inside block 200, the signal passes through two inverters, INV1 and INV2, and then into a CMOS inverter structure. This structure consists of a PMOS transistor (PM1) and an NMOS transistor (NM1) in series, and another PMOS transistor (PM2) and NMOS transistor (NM2) in series. The gates of PM1 and NM2 are connected to the input of the block, while the gates of PM2 and NM1 are connected to the output of the block, forming a feedback loop. The output of the block is connected to a third inverter, INV3, which is followed by a fourth inverter, INV4, leading to the final output driving unit.